WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a semiconductor circuit which is formed inside of said semiconductor device; and

an electrode structure which is formed on a first surface of the semiconductor device,

said electrode structure including a first electrode layer and a metal plating layer which is formed on said first electrode layer, said first electrode layer being formed of a first metal and connected to said semiconductor circuit, said metal plating layer being formed of a second metal, and said second metal being capable of being soldered onto an extraction electrode outside of said semiconductor device.

2. A semiconductor device according to claim 1, which further comprises a protective film which is formed on said first surface,

wherein said metal plating layer is selectively formed in a region of said first electrode layer by using said protective film as a mask.

3. A semiconductor device according to claim 1, wherein said first metal is AL (aluminum), and said first electrode layer has a thickness of 0.5 μm or more.

4. A semiconductor device according to claim 2, wherein said first metal is AL (aluminum), and said first electrode layer has a thickness of 0.5 μm or more.

5. A semiconductor device according to claim 1, wherein said metal plating layer is formed by a wet electroless plating.

6. A semiconductor device according to claim 1, wherein said second metal includes at least one of Ni (nickel) and Cu (copper).

7. A semiconductor device according to claim 2, wherein said protective film is formed of PI (polyimide resin).

8. A semiconductor device according to claim 1, wherein said semiconductor device is a MOS type high power semiconductor device which further comprises a second electrode layer which is formed of a third metal on a second surface which is the opposite surface to said first surface,

said first electrode layer forms at least one electrode of gate and source electrodes, and

said second electrode layer forms a drain electrode.

9. A package for semiconductor device comprising:

a semiconductor device including a semiconductor circuit and an electrode structure, said semiconductor circuit being formed inside of said semiconductor device, said electrode structure being formed on a first surface of said semiconductor device and having a first electrode layer and a metal plating layer which is formed on said first electrode layer,

said first electrode layer being formed of a first metal and connected to said semiconductor circuit,

said metal plating layer being formed of a second metal, said second metal being capable of being soldered onto an extraction electrode outside of said semiconductor device;

a supporting substrate which supports thereon said semiconductor device;

a lead terminal which is formed of a third metal and connected to said first electrode layer; and

a metal plate which is formed of a fourth metal to serve as said extraction electrode and which connects said lead terminal to said first electrode layer via said metal plating layer.

10. A package for semiconductor device according to claim 9, which further comprises a protective film which is formed on said first surface,

wherein said metal plating layer is selectively formed in a region of said first electrode layer by using said protective film as a mask.

11. A package for semiconductor device according to claim 9, wherein said first metal is AL (aluminum), and said first electrode layer has a thickness of 0.5 μm or more.

12. A package for semiconductor device according to claim 9, wherein said metal plating layer is formed by a wet electroless plating.

13. A package for semiconductor device according to claim 9, wherein said second metal includes at least one of Ni (nickel) and Cu (copper).

14. A package for semiconductor device according to claim 10, wherein said protective film is formed of PI (polyimide resin).

15. A package for semiconductor device comprising:

a MOS type high power semiconductor device including a semiconductor circuit and an electrode structure, said semiconductor circuit being formed inside of said semiconductor device, said electrode structure being formed on a first surface of said semiconductor device and having a first electrode layer, a metal plating layer and a second electrode layer,

said first electrode layer being formed of a first metal and connected to said semiconductor circuit, said metal plating layer being formed of a second metal on said first electrode layer, said second electrode layer being formed of a third metal on a second surface which is the opposite surface to said first surface, said second metal being capable of being soldered onto an extraction electrode outside of said semiconductor device, said first electrode layer and said metal plating layer forming at least one electrode of gate and source electrodes, and said second electrode layer forming a drain electrode;

a frame plate which is formed of a fourth metal, supports said semiconductor device on said second surface of said semiconductor device and is connected to said second electrode

layer;

a lead terminal which is formed of a fifth metal and is connected to said first electrode layer; and

a metal plate which is formed of a sixth metal to serve as said extraction electrode and which connects said lead terminal to said first electrode layer via said metal plating layer.

16. A package for semiconductor device according to claim 15, which further comprises a protective film which is formed on said first surface,

wherein said metal plating layer is selectively formed in a region of said first electrode layer by using said protective film as a mask.

17. A package for semiconductor device according to claim 15, wherein said first metal is AL (aluminum), and said first electrode layer has a thickness of 0.5 μm or more.

18. A package for semiconductor device according to claim 15, wherein said metal plating layer is formed by a wet electroless plating.

19. A package for semiconductor device according to claim 15, wherein said second metal includes at least one of Ni (nickel) and Cu (copper).

20. A package for semiconductor device according to claim 16, wherein said protective film is formed of PI (polyimide resin).